1. Communication circuitry comprising:

parallel channels configured to transfer communications in parallel with a clock signal;

processing circuitry configured to exchange the communications between communication links and the parallel channels; and

crossbar integrated circuits configured to receive the communications and the clock signal over the parallel channels, switch the communications based on the clock signal, and transfer the switched communications to the parallel channels.

2. The communication circuitry of claim 1 wherein the parallel channels are each comprised of parallel differential signal pairs wherein one of the differential signal pairs is for the clock signal.

3. The communication circuitry of claim 1 wherein the communication links comprise serial channels.

4. The communication circuitry of claim 1 wherein the communications comprise data packets.

5. The communication circuitry of claim 1 wherein the communications comprise fixed-length data packets.

6. The communication circuitry of claim 1 wherein the communication circuitry comprises a switch fabric.

7. The communication circuitry of claim 1 wherein the processing circuitry is comprised of virtual output queues that store the communications prior to switching and that are associated with egress ports.

8. The communication circuitry of claim 1 wherein the processing circuitry is comprised of virtual output queues that store the communications prior to switching and wherein each virtual output queue is comprised of sub-queues that are each associated with a different priority.

9. The communication circuitry of claim 1 wherein the processing circuitry is comprised of a multi-cast virtual output queue that stores the communications prior to switching for multi-cast output.

10. The communication circuitry of claim 1 wherein the parallel channels include multiplexers to perform bit slicing through the crossbar integrated circuits.

11. A method of operating communication circuitry, the method comprising:

exchanging communications between communication links and processing circuitry;

exchanging the communications and a clock signal between the processing circuitry and parallel channels;

transferring the communications in parallel with the clock signal over the parallel channels;

receiving the communications and the clock signal from the parallel channels into crossbar integrated circuits;

switching the communications in the crossbar integrated circuits based on the clock signal, and

transferring the switched communications from the crossbar integrated circuits to the parallel channels.

12. The method of claim 11 wherein transferring the communications in parallel with the clock signal comprises transferring the communications and the clock signal over parallel differential signal pairs wherein one of the differential signal pairs is for the clock signal.

13. The method of claim 11 wherein exchanging the communications between the communication links and the processing circuitry comprises exchanging the communications between serial channels and the processing circuitry.

14. The method of claim 11 wherein the communications comprise data packets.

15. The method of claim 11 wherein the communications comprise fixed-length data packets.

16. The method of claim 11 wherein the communication circuitry comprises a switch fabric.

17. The method of claim 11 further comprising, in the processing circuitry, storing the communications in virtual output queues that are associated with egress ports prior to switching.

18. The method of claim 11 further comprising, in the processing circuitry, storing the communications in virtual output sub-queues that are each associated with a different priority.

19. The method of claim 11 further comprising, in the processing circuitry, storing the communications in a multicast virtual output queue that stores the communications prior to switching for multi-cast output.

20. The method of claim 11 wherein transferring the communications in parallel with the clock signal comprises multiplexing the communications to perform bit slicing through the crossbar integrated circuits.